controller, which transfers m bits of data in parallel; and

a second bus, having n (wherein n is an integer, n > m) bits width, connected between said memory controller and said data processor, which transfers n bits of data in parallel;

wherein said memory controller comprises:

a storage which temporarily stores graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said first bus,

a circuit which forms n bits of data using said successive groups of m bits of data and supplies said n bits of data in parallel to said data processor through said second bus based on an indication from said data processor, and

B1 Cont

a converter which converts said graphic data temporarily stored in said storage into serial data which is provided to said DAC based on an indication from said data processor.

10. (Amended) An apparatus according to claim 9, wherein said memory controller further comprises:

a multiplexer which outputs the n bits graphic data transferred from said data processor to said first bus having m bits width in a time shared fashion.

11. (Amended) An apparatus according to claim 9, wherein said memory controller further comprises:

a second circuit which generates an address signal for accessing said memory plural times, in response to a signal for accessing said memory supplied from said data processor.

B1 Cont

~~14.~~ 14 (Amended) A graphic processing apparatus comprising:

a memory which stores graphic data;

a data processor which executes predetermined graphic processing to generate graphic data;

a memory controller which controls transfer of data between said memory and said data processor in response to a request from said data processor;

B2 Cont

a digital to analog converter (DAC), connected to said memory controller, which outputs said graphic data read out from said memory;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory and said memory controller, which transfers data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processor, which transfers data of n bits in parallel,

wherein said memory controller includes:

a storage which temporarily stores graphic data read out from said memory successively in a predetermined period of time via said first bus,

a circuit which applies said temporarily stored graphic data to said data processor as n-bit parallel data based on an indication from said data processor, and

a converter which converts said temporarily stored graphic data into serial data and outputs the serial data to said DCA based on an indication from said data processor.

~~15.~~ 15. (Amended) A graphic processing apparatus according to claim ~~14~~ 14, wherein said memory controller includes a multiplexer which outputs n-bit graphic data transferred from said data processor on said first bus having the m-bit width successively in a time-sharing manner.

B2 Cont

~~16.~~ 19. (Amended) A graphic processing apparatus according to claim ~~14~~ 14, wherein said memory controller includes a second circuit which generates address signals for accessing said memory plural times with respect to a signal for accessing said memory applied from said data processor.

~~17.~~ 16. (Amended) A graphic processing apparatus according to claim ~~15~~ 15, wherein said memory controller includes a second circuit which generates address signals for accessing said memory plural times with respect to a signal for accessing said memory means applied from said data processor.

~~18.~~ 20. (Amended) A graphic processing apparatus according to claim ~~14~~ 14, wherein graphic data to be transferred to said

memory controller via said first bus are successively read out plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to said memory designated by said data processor.

~~19.~~ 17. (Amended) A graphic processing apparatus according to claim ~~15~~, wherein graphic data to be transferred to said memory controller via said first bus are successively read out plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to said memory designated by said data processor.

B2 cont

~~20.~~ 21. (Amended) A graphic processing apparatus according to claim ~~18~~, wherein graphic data transferred to said memory controller are applied to said data processor via said second bus within a time period more than two times said transfer unit time.

~~21.~~ 18. (Amended) A graphic processing apparatus according to claim ~~19~~, wherein graphic data transferred to said memory controller are applied to said data processor via said second bus within a time period more than two times said transfer unit time.

~~22.~~ 22. (Amended) A graphic processing apparatus comprising:

a memory which stores graphic data, said memory being accessed by using a row address and a column address;

a data processor which executes predetermined graphic processing to generate graphic data;

a memory controller which controls transfer of data between said memory and said data processor in response to a request from said data processor;

a digital to analog converter (DAC), connected to said memory controller, which outputs said graphic data read out from said memory;

B7 cont

a first bus having an m-bit width (wherein m is an integer) and connected between said memory and said memory controller, which transfers data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processor, which transfers data of n bits in parallel; and

wherein said memory controller includes:

a first circuit which reads out a plurality of graphic data at different column addresses at a same row address from said memory via said first bus successively in a predetermined period of time,

a second circuit which applies said read-out graphic data to said data processor as n-bit parallel data based on an indication from said data processor, and

a converter which converts said read-out graphic data into serial data and outputs the serial data to said DAC based on an indication from said data processor.

15 23

23. (Amended) A graphic processing apparatus according to claim 14 22, wherein said memory controller includes a third circuit which successively generates a plurality of column addresses based on a signal for accessing said memory applied from said data processor.

16 24

24. (Amended) A memory controller for controlling transference of data between a memory and a processor, said memory controller comprising:

B2 cont

m bit terminals for coupling to said memory, wherein successive groups of m bits of data is transferred through said m bit terminals between said memory and said controller by performing plural read operations within a memory cycle (where m is an integer);

n bit terminals for coupling to said processor, wherein n bits of data is transferred in parallel through said n bit terminals between said controller and said processor (where n is an integer and n>m);

a storage which temporarily stores graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said m bit terminals;

a first circuit which forms n bits of data by combining successive groups of m bits of data from said m bit terminals and supplies said n bits of data in parallel to said n bit terminals based on an indication from said processor; and

a converter which converts said graphic data temporarily stored in said storage into serial data which is supplied to a digital to analog converter (DAC), said DAC being connected to said memory controller.

Please add new claims 28-46 as follows:

-- ~~20~~ 28. A graphic processing apparatus comprising:

a memory which stores graphic data;

a data processor which executes a predetermined graphic processing to generate graphic data to be stored in said memory;

a memory controller which controls data transfer between said memory and said data processor in accordance with a request from said data processor;

a first bus, having m (wherein m is an integer) bits width, connected between said memory and said memory controller, which transfers m bits of data in parallel; and

a second bus, having n (wherein n is an integer, n > m) bits width, connected between said memory controller and said data processor, which transfers n bits of data in parallel;

wherein said memory controller comprises:

at least one output terminal;

a storage which temporarily stores graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said first bus,

a circuit which forms n bits of data using said successive groups of m bits of data and supplies said n bits of data in parallel to said data processor through said second bus based on an indication from said data processor, and

a converter which converts said graphic data temporarily stored in said storage into serial data which is provided to said at least one output terminal based on an indication from said data processor.

~~27~~ 29. An apparatus according to claim ~~26~~ 28, wherein said memory controller further comprises:

a multiplexer which outputs the n bits graphic data transferred from said data processor to said first bus having m bits width in a time shared fashion.

~~28~~ 30. An apparatus according to claim ~~25~~ 28, wherein said memory controller further comprises:

a second circuit which generates an address signal for accessing said memory plural times, in response to a signal for accessing said memory supplied from said data processor.

~~29~~ 31. An apparatus according to claim ~~26~~ 28, wherein graphic data to be transferred to said memory controller through said first bus is read out from said memory plural times within a unit transfer time in a time shared fashion, based on an

access signal to said memory designated by said data processor.

24 32. An apparatus according to claim 23 31, wherein the graphic data transferred to said memory controller is supplied to said data processor through said second bus within a time longer than twice said unit transfer time.

25 33. A graphic processing apparatus comprising:

a memory which stores graphic data;

a data processor which executes predetermined graphic processing to generate graphic data;

a memory controller which controls transfer of data between said memory and said data processor in response to a request from said data processor;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory and said memory controller, which transfers data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processor, which transfers data of n bits in parallel,

wherein said memory controller includes:

at least one output terminal;

a storage which temporarily stores graphic data read out from said memory successively in a predetermined period of time via said first bus,

a circuit which applies said temporarily stored graphic data to said data processor as n-bit parallel data based on an indication from said data processor, and

a converter which converts said temporarily stored graphic data into serial data and outputs the serial data to said at least one output terminal based on an indication from said data processor.

34. A graphic processing apparatus according to claim 33, wherein said memory controller includes a multiplexer which outputs n-bit graphic data transferred from said data processor on said first bus having the m-bit width successively in a time-sharing manner.

35. A graphic processing apparatus according to claim 33, wherein said memory controller includes a second circuit which generates address signals for accessing said memory plural times with respect to a signal for accessing said memory applied from said data processor.

36. A graphic processing apparatus according to claim 34, wherein said memory controller includes a second circuit which generates address signals for accessing said memory plural times with respect to a signal for accessing said memory means applied from said data processor.

~~37~~ 39. A graphic processing apparatus according to claim ~~33~~ 25, wherein graphic data to be transferred to said memory controller via said first bus are successively read out plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to said memory designated by said data processor.

~~28~~ 36. A graphic processing apparatus according to claim ~~34~~ 34, wherein graphic data to be transferred to said memory controller via said first bus are successively read out plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to said memory designated by said data processor.

~~39~~ 40. A graphic processing apparatus according to claim ~~37~~ 31, wherein graphic data transferred to said memory controller are applied to said data processor via said second bus within a time period more than two times said transfer unit time.

~~40~~ 37. A graphic processing apparatus according to claim ~~38~~ 36, wherein graphic data transferred to said memory controller are applied to said data processor via said second bus within a time period more than two times said transfer unit time.

~~41~~ 41. A graphic processing apparatus comprising:

a memory which stores graphic data, said memory being accessed by using a row address and a column address;

a data processor which executes predetermined graphic processing to generate graphic data;

a memory controller which controls transfer of data between said memory and said data processor in response to a request from said data processor;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory and said memory controller, which transfers data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processor, which transfers data of n bits in parallel; and

wherein said memory controller includes:

at least one output terminal;

a first circuit which reads out a plurality of graphic data at different column addresses at a same row address from said memory via said first bus successively in a predetermined period of time,

a second circuit which applies said read-out graphic data to said data processor as n-bit parallel data based on an indication from said data processor, and

a converter which converts said read-out graphic data into serial data and outputs the serial data to said at least one output terminal based on an indication from said data processor.

~~34~~ 42 ~~42~~. A graphic processing apparatus according to claim ~~33~~ 41 ~~41~~, wherein said memory controller includes a third circuit which successively generates a plurality of column addresses based a signal for accessing said memory applied from said data processor.

~~35~~ 43 ~~43~~. A memory controller for controlling transference of data between a memory and a processor, said memory controller comprising:

m bit terminals for coupling to said memory, wherein successive groups of m bits of data is transferred through said m bit terminals between said memory and said controller by performing plural read operations within a memory cycle (where m is an integer);

n bit terminals for coupling to said processor, wherein n bits of data is transferred in parallel through said n bit terminals between said controller and said processor (where n is an integer and n>m);

a storage which temporarily stores graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said m bit terminals;

a first circuit which forms n bits of data by combining successive groups of m bits of data from said m bit terminals and supplies said n bits of data in parallel to said n bit terminals based on an indication from said processor; and